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10/073,241	02/13/2002	Marko Karppanen	60279.00138	8874

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SQUIRE, SANDERS & DEMPSEY L.L.P.
14TH FLOOR
8000 TOWERS CRESCENT
TYSONS CORNER, VA 22182

EXAMINER	
MCCARTHY, CHRISTOPHER S	
ART UNIT	**PAPER NUMBER**
2113	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/073,241	KARPPANEN, MARKO	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-18,20-26 and 29-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-18,20-26 and 29-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *response to arguments*.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 9-16, 20-23, 25,29-30, 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Golikeri et al. U.S. Patent Application Publication US2003/0067926.

As per claim 9, Golikeri teaches a method for improving the reliability of a computer system including a bus, at least one plug-in unit and at least one separate interface circuit corresponding to each of the at least one plug in unit (¶ 0051), comprising: connecting at least one plug-in unit to the bus via the separate interface circuit (¶ 0051, 0071-0072, wherein, modules can be added or removed without powering off; this is interpreted as hot-plugging and, therefore, plug in units; 0036, wherein, a bus is described as connecting the modules; 0050-0051, wherein, interface logic is described in the form of the management/control logic unit of the module that controls, monitors the other components and is responsible for the connection and operation of the module, and, therefore, the addressing operations of the module); addressing a respective plug-in unit, via the bus, by addressing operations directed at said respective plug-in

unit and which are monitored locally by said interface circuit corresponding thereto (¶ 0051, wherein the operations are controlled by the management/control interface; 0018, wherein, it is taught that the local addressing operations of the module are monitored locally); performing a time duration operation of addressing of said plug-in unit (¶ 0060-0061); and checking the state of addressing of the addressed plug-in unit such that (i) when the addressing is ended before expiration of a predetermined period of time, the time duration operation of addressing is terminated and a new time duration operation of addressing is set to commence at time of next occurrence of addressing (¶ 0060, wherein, when the timer is reset when the module processes a data frame before the timer expires), and (ii) when the duration operation of addressing exceeds the predetermined time period, the addressing to that plug-in unit is terminated by the interface circuit by sending into the bus a signal indicating termination of addressing (¶ 0039, 0060-0061, wherein, the local addressing operation of the module times out and a signal is sent out on the bus/network that the corresponding address is now obsolete, that is, no longer valid, erroneous).

As per claim 10, Golikeri teaches teaches a method as defined in claim 9, wherein: the time duration of addressing is monitored using a watchdog timer with a predetermined timing set therein (¶ 0060).

As per claim 11, Golikeri teaches a method as defined in claim 9, wherein: when addressing is terminated an error signal is set by the interface circuit into an active state in the bus (¶ 0061, wherein, the purge signal set to active to be sent over the bus/network).

As per claim 12, Golikeri teaches a method as defined in claim 9, wherein: when addressing is terminated an error signal indicating an error condition in the plug-in unit is set by the interface circuit into active state in the status register of the plug-in unit (¶0040, 0041;

wherein, the status of the register is changed in that the module will no longer send out "keep-live" messages to other modules, so they will know that the address was purged; just in case the purge message was not received by all other modules).

As per claim 13, Golikeri teaches an interface circuit for providing local monitoring capability to a plug-in unit of a computer, comprising: a watchdog timer (P 0060-0061); first means for activating the watchdog timer upon start of an addressing operation directed to the plug-in unit corresponding thereto (¶0060, wherein, the aging timer must have been started prior to the expiration thereof), and second means for sending into the bus a signal indication termination of addressing, the termination of addressing being effected when the duration of said addressing exceeds a predetermined time duration for addressing, as measured by the watchdog timer (¶0060-0061).

As per claim 14, Golikeri teaches an interface circuit as defined in claim 13, further comprising: means for setting an error signal into active state in the bus (¶ 0061).

As per claim 15, Golikeri teaches an interface circuit as defined in 13, further comprising: for setting a signal indicating an error condition in the plug-in unit into an active state in the status register of the plug-in unit (P 0040, 0041; wherein, the status of the register is changed in that the module will no longer send out "keep-live" messages to other modules, so they will know that the address was purged; just in case the purge message was not received by all other modules).

As per claim 16, Golikeri teaches an interface circuit as defined in 14, further comprising: means for setting a signal indicating an error condition in a plug-in unit into an active state in the status register of the plug-in unit (P 0040, 0041; wherein, the status of the register is inherently

changed in that the module will no longer send out "keep-live" messages to other modules, so they will know that the address was purged; just in case the purge message was not received by all other modules).

As per claim 20, Golikeri teaches a method according to claim 10, wherein: said watchdog timer is provided at said interface circuit (¶ 0060-0061; 0051, wherein the logic interface is taught as to control the switching module).

As per claim 21, Golikeri teaches a computer system including a bus, at least one plug-in unit and at least one separate interface circuit corresponding to each of the at least one plu g in unit (¶0051), wherein the improvement comprises: at least one separate interface circuit correspond to each of the at least one plug in unit where each plug in unit is connected to said bus via the separate said interface circuit (¶ 0071-0072, 0036, 0050-0051), wherein each said interface circuit comprises a watchdog timer (¶ 0060), first means for activating the watchdog timer upon start of an addressing operation directed to the corresponding plug-in unit (¶ 0060, wherein, activation of said timer must have been prior to the detection of whether the timer has expired), and second means for sending into the bus a signal indicating termination of addressing, the termination of addressing being effected when the duration of said addressing exceeds a predetermined time duration for addressing, as measured by the watchdog timer (¶ 0060-0061).

As per claim 22, Golikeri teaches a computer system according to claim 21, wherein each said interface further comprises: means for setting an error signal into an active state in the bus (¶ 0061).

As per claim 23, Golikeri teaches a computer system according to claim 22, wherein each said interface circuit comprises means for setting a signal indicating an error condition in the corresponding plug-in unit into an active state in a status register of the plug-in unit (P 0040, 0041; wherein, the status of the register is inherently changed in that the module will no longer send out "keep-live" messages to other modules, so they will know that the address was purged,; just in case the purge message was not received by all other modules).

As per claim 25, Golikeri teaches a computer system according to claim 21, wherein each said interface circuit comprises means for setting a signal indicating an error condition in the plug-in unit into an active state in a status register of the plug-in unit (P 0040, 0041; wherein, the status of the register is inherently changed in that the module will no longer send out "keep-live" messages to other modules, so they will know that the address was purged; just in case the purge message was not received by all other modules).

As per claim 29, Golikeri teaches an interface circuit for providing local monitoring capability to a plug-in unit of a computer system, comprising a bus and plug-in units connected to the bus ¶ 0036) via a separate interface circuits, thereby connecting each plug-in unit to the bus (¶ 0050-0051); a watchdog timer ¶ 0060); an activating device configured to activate the watchdog timer upon start of an addressing operation directed to the corresponding plug-in unit (¶ 0060-0061, wherein, activation of the timer must have been achieved prior to detection of the timer expiration); and a sending device configured to send a signal into the bus indicating termination of addressing, the termination of addressing being effected when the duration of said addressing exceeds a predetermined time duration for addressing, as measured by the watchdog timer (¶ 0061).

As per claim 30, Golikeri teaches an interface circuit as defined in claim 29, further comprising a device configured to set a signal indicating an error condition in a plug-in unit into an active state in a status register of the plug-in unit ((P 0040, 0041; wherein, the status of the register is changed in that the module will no longer send out "keep-live" messages to other modules, so they will know that the address was purged; just in case the purge message was not received by all other modules).

As per claim 33, Golikeri teaches an interface circuit as defined in claim 29, further comprising a device for setting an error signal into an active state in a bus (¶ 0061).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 17-18, 24, 26, 28, 31, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Golikeri in view of Microsoft Computer Dictionary, referred hereon as Microsoft.

As per claim 17, Golikeri teaches an interface circuit as defined in claim 13 with a bus (¶ 0036). Golikeri does not explicitly teach wherein the bus is a CompactPCI bus. Microsoft does

teach a CompactPCI bus (page 99). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the CompactPCI bus of Microsoft in the bus system of Golikeri. One of ordinary skill would have been motivated to use the CompactPCI bus of Microsoft in the bus system of Golikeri because Microsoft teaches wherein the CompactPCI bus is suitable for high-speed communication devices, such as router; this is an explicit embodiment of Golikeri (¶ 0088), and a high speed communication means would have been a desired advantage in Golikeri in that he teaches the desire of multiple connected peripheral modules, such as routers, in strict synchronization with another.

As per claim 18, Golikeri teaches an interface circuit as defined in claim 16 with a bus (¶ 0036). Golikeri does not explicitly teach wherein the bus is a CompactPCI bus. Microsoft does teach a CompactPCI bus (page 99). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the CompactPCI bus of Microsoft in the bus system of Golikeri. One of ordinary skill would have been motivated to use the CompactPCI bus of Microsoft in the bus system of Golikeri because Microsoft teaches wherein the CompactPCI bus is suitable for high-speed communication devices, such as router; this is an explicit embodiment of Golikeri (¶ 0088), and a high speed communication means would have been a desired advantage in Golikeri in that he teaches the desire of multiple connected peripheral modules, such as routers, in strict synchronization with another.

As per claim 24, Golikeri teaches a computer system according to claim 23, with a bus (¶ 0036). Golikeri does not explicitly teach wherein the bus is a CompactPCI bus. Microsoft does teach a CompactPCI bus (page 99). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the CompactPCI bus of Microsoft in the bus system of

Golikeri. One of ordinary skill would have been motivated to use the CompactPCI bus of Microsoft in the bus system of Golikeri because Microsoft teaches wherein the CompactPCI bus is suitable for high-speed communication devices, such as router; this is an explicit embodiment of Golikeri (¶ 0088), and a high speed communication means would have been a desired advantage in Golikeri in that he teaches the desire of multiple connected peripheral modules, such as routers, in strict synchronization with another.

As per claim 26, Golikeri teaches a computer system according to claim 21, with a bus (¶ 0036). Golikeri does not explicitly teach wherein the bus is a CompactPCI bus. Microsoft does teach a CompactPCI bus (page 99). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the CompactPCI bus of Microsoft in the bus system of Golikeri. One of ordinary skill would have been motivated to use the CompactPCI bus of Microsoft in the bus system of Golikeri because Microsoft teaches wherein the CompactPCI bus is suitable for high-speed communication devices, such as router; this is an explicit embodiment of Golikeri (¶ 0088), and a high speed communication means would have been a desired advantage in Golikeri in that he teaches the desire of multiple connected peripheral modules, such as routers, in strict synchronization with another.

As per claim 28, Golikeri teaches a computer system according to claim 27, with a bus (¶ 0036). Golikeri does not explicitly teach wherein the bus is a CompactPCI bus. Microsoft does teach a CompactPCI bus (page 99). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the CompactPCI bus of Microsoft in the bus system of Golikeri. One of ordinary skill would have been motivated to use the CompactPCI bus of Microsoft in the bus system of Golikeri because Microsoft teaches wherein the CompactPCI bus

is suitable for high-speed communication devices, such as router; this is an explicit embodiment of Golikeri (¶ 0088), and a high speed communication means would have been a desired advantage in Golikeri in that he teaches the desire of multiple connected peripheral modules, such as routers, in strict synchronization with another.

As per claim 31, Golikeri teaches a computer system according to claim 29, with a bus (¶ 0036). Golikeri does not explicitly teach wherein the bus is a CompactPCI bus. Microsoft does teach a CompactPCI bus (page 99). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the CompactPCI bus of Microsoft in the bus system of Golikeri. One of ordinary skill would have been motivated to use the CompactPCI bus of Microsoft in the bus system of Golikeri because Microsoft teaches wherein the CompactPCI bus is suitable for high-speed communication devices, such as router; this is an explicit embodiment of Golikeri (¶ 0088), and a high speed communication means would have been a desired advantage in Golikeri in that he teaches the desire of multiple connected peripheral modules, such as routers, in strict synchronization with another.

As per claim 32, Golikeri teaches a computer system according to claim 30, with a bus (¶ 0036). Golikeri does not explicitly teach wherein the bus is a CompactPCI bus. Microsoft does teach a CompactPCI bus (page 99). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the CompactPCI bus of Microsoft in the bus system of Golikeri. One of ordinary skill would have been motivated to use the CompactPCI bus of Microsoft in the bus system of Golikeri because Microsoft teaches wherein the CompactPCI bus is suitable for high-speed communication devices, such as router; this is an explicit embodiment of Golikeri (¶ 0088), and a high speed communication means would have been a desired

advantage in Golikeri in that he teaches the desire of multiple connected peripheral modules, such as routers, in strict synchronization with another.

Response to Arguments

3. Applicant's arguments filed 1/11/07 have been fully considered but they are not persuasive.

The applicant has amended the claims to include the language of "of at least one separate interface circuit corresponding to each of the at least one plug-in unit"; and has argued that this limitation overcomes Golikeri. The examiner respectfully disagrees. The new language is not particularly distinct from past arguments. The examiner would like to reiterate the teaching and interpretation of Golikeri as it applies to the limitation. In paragraph 0051, Golikeri states "The management/control logic (115, 125, 135) *interfaces* with other components of the Ethernet switching module (110, 120, 130) in order to manage and control the operations of the Ethernet switching module..."(emphasis added). So the interpretation of the reading by the examiner is that the management/control logic is the interface of the module (unit); therefore, each module has a corresponding interface that is responsible for the local monitoring and control of the respective module.

As per claim 13, the applicant argues the existing language of activating a watchdog timer upon startup of an addressing operation Is not taught in Golikeri. The examiner respectfully disagrees. As cite in rejection, paragraph 0060 teaches that a timer is reset upon a command to process a local address. This is deemed as starting a timer upon an address operation. Also, the applicant argues that Golikeri does not teach sending a signal on a bus

indicating termination of the addressing process when the timer expires. The examiner respectfully disagrees. As cited in the rejection, Golikeri teaches in paragraphs 0060-0061 that when the timer expires, a purge message is sent to other modules over a bus. This is deemed as a signal sent over a bus when an addressing operation has expired.

The applicant is urged to more clearly map out arguments in the next response to point out what claim language is not taught in Golikeri and then cite passages in Golikeri that perhaps teaches away or fails to teach the limitations. Re-writing the whole claim language and then saying Golikeri doesn't teach the language is not effective in itself.

In light of the arguments above, all applicable claims stand rejected.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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